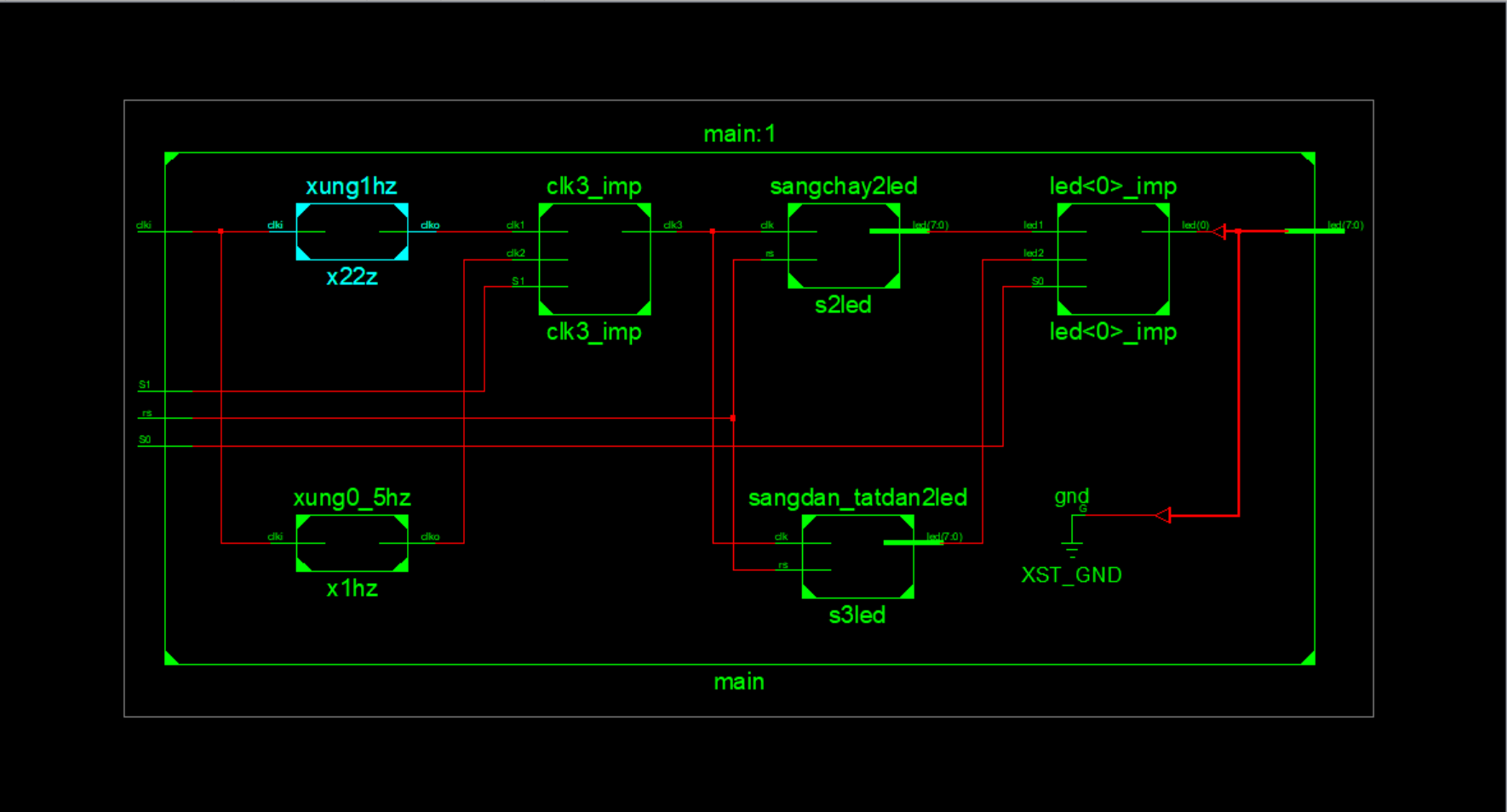
Nguyễn Phước Dư – 21119327

1. Thiết kế logic:



1. Mô tả phần cứng

module sangchay2led(

input wire clk,

input wire rs,

output wire [7:0]led

);

reg [7:0]d;

always @(posedge clk or posedge rs) begin

if (rs) begin

d<= 8'b00000011;

end else begin

d <= {d[6:0],d[7]};

end

end

assign led = d;

endmodule

module sangdan\_tatdan2led(

input wire clk,

input wire rs,

output wire [7:0]led

);

reg [7:0]d;

always @(posedge clk or posedge rs) begin

if (rs) begin

d<= 8'b00000011;

end else begin

d <= {d[6:0],d[7]};

end

end

assign led = d;

endmodule

module xung0\_5hz(

input wire clki,

output reg clko

);

wire [40:0] r\_next ;

reg [40:0] r\_reg;

initial

begin

r\_reg =0 ;

clko = 0;

end

always @(posedge clki) begin

r\_reg = r\_next;

if (r\_reg==50000000) clko = ~clko;

end

assign r\_next =(r\_reg==100000000)?0: r\_reg + 1 ;

//assign clk\_hz = r\_reg[26];// =(r\_reg<=50000000/2)?0:1;

endmodule

module xung1hz(

input wire clki,

output reg clko

);

wire [40:0] r\_next ;

reg [40:0] r\_reg;

initial

begin

r\_reg =0 ;

clko = 0;

end

always @(posedge clki) begin

r\_reg = r\_next;

if (r\_reg==12500000) clko = ~clko;

end

assign r\_next =(r\_reg==25000000)?0: r\_reg + 1 ;

//assign clk\_hz = r\_reg[26];// =(r\_reg<=50000000/2)?0:1;

endmodule

module main(

input clki,S0,S1,

input rs,

output reg[7:0]led

);

wire clk1,clk2;

reg clk3;

wire led1,led2;

xung1hz x22z(clki,clk1);

xung0\_5hz x1hz(clki,clk2);

always @\* begin

if (S1==1) clk3=clk1;

else clk3=clk2;

end

sangchay2led s2led(clk3,rs,led1);

sangdan\_tatdan2led s3led(clk3,rs,led2);

always @\* begin

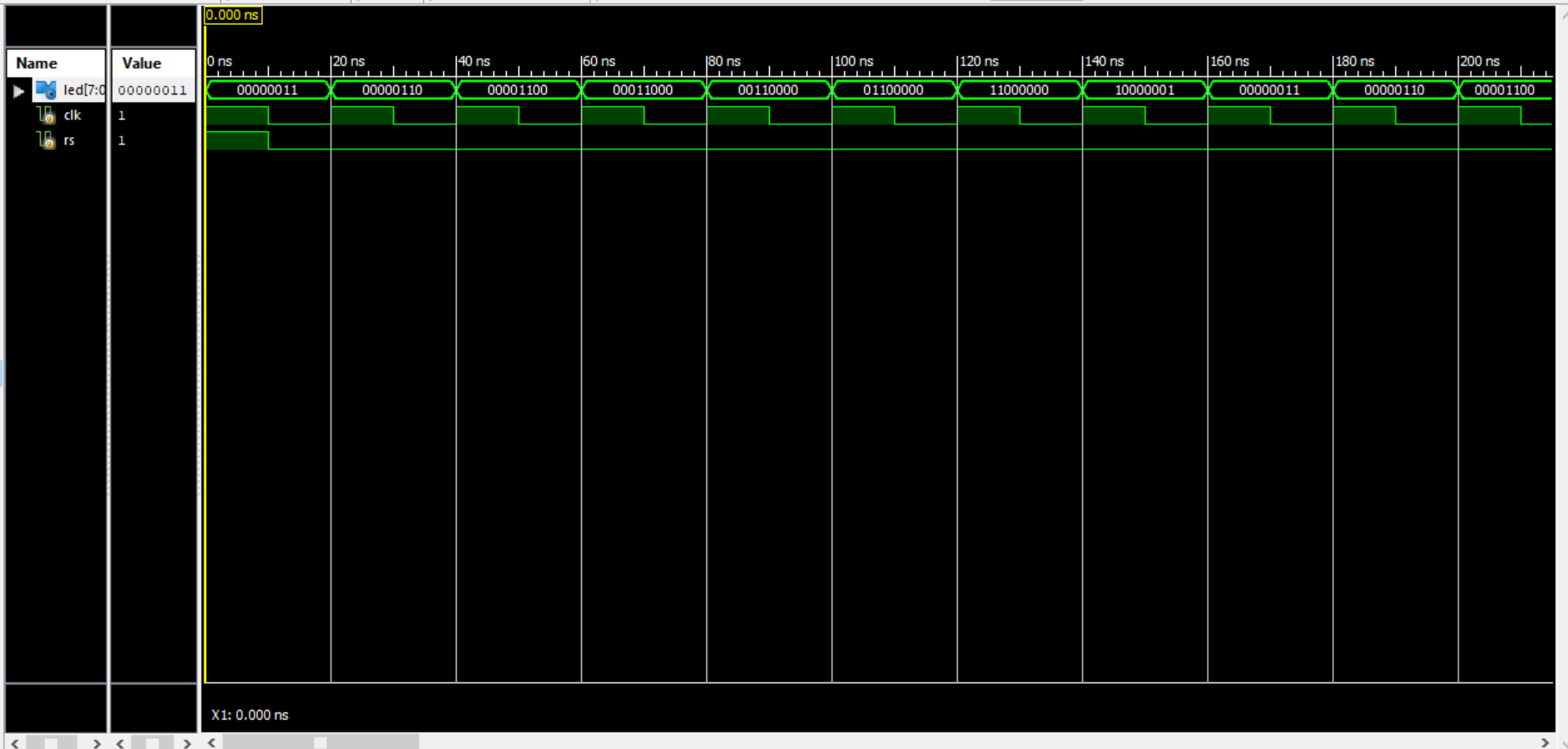
if (S0==1) led=led1;

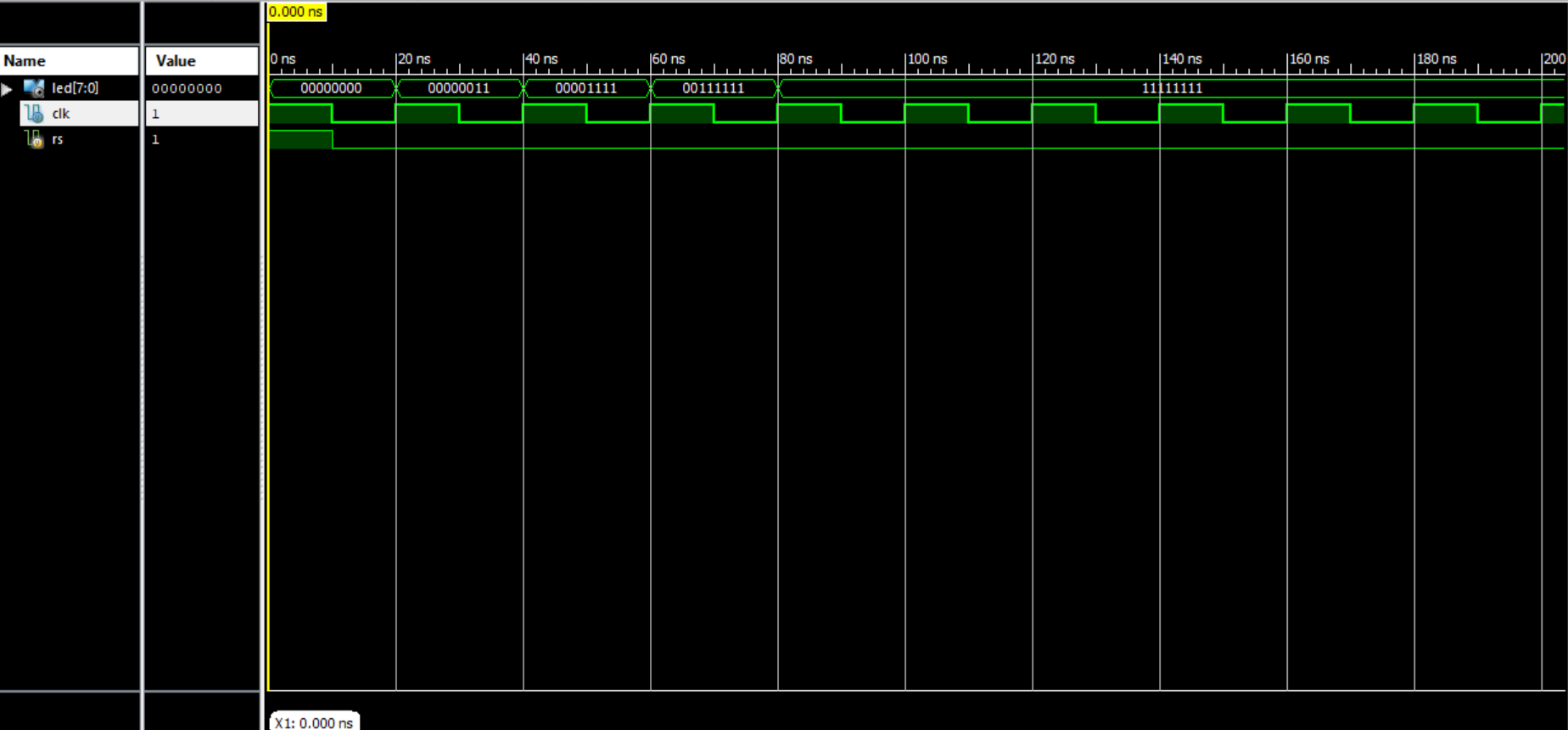
else led=led2;

end

endmodule

1. Mô phỏng





1. Kết nối phần cứng